**Kyle Ward**

**Single-Cycle CPU Datapath Elements**

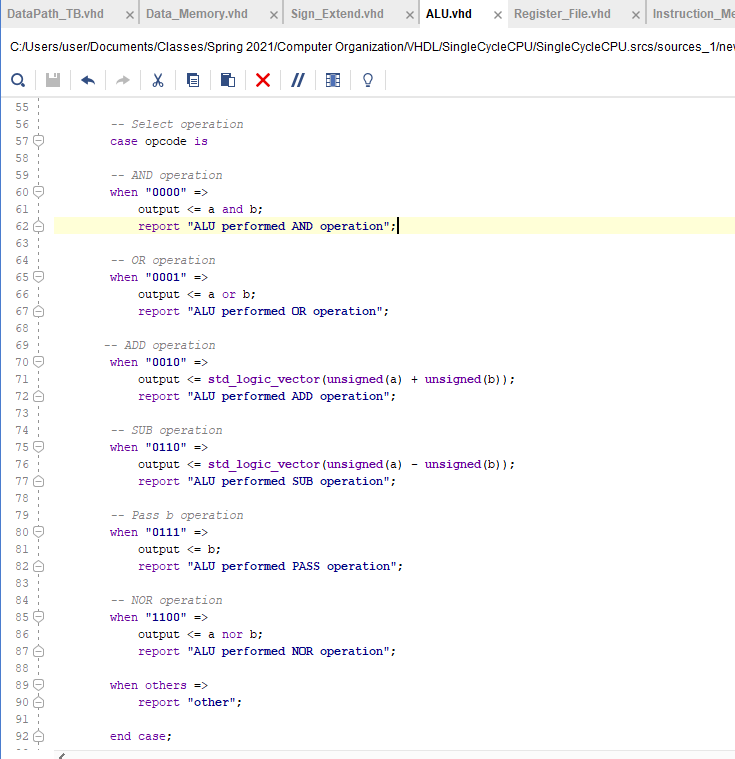


Figure 1. Arithmetic Logic Unit

* In the figure above you can see the vhdl code for my ALU. It uses a switch-case statement to determine which operation to perform based on the opcode input

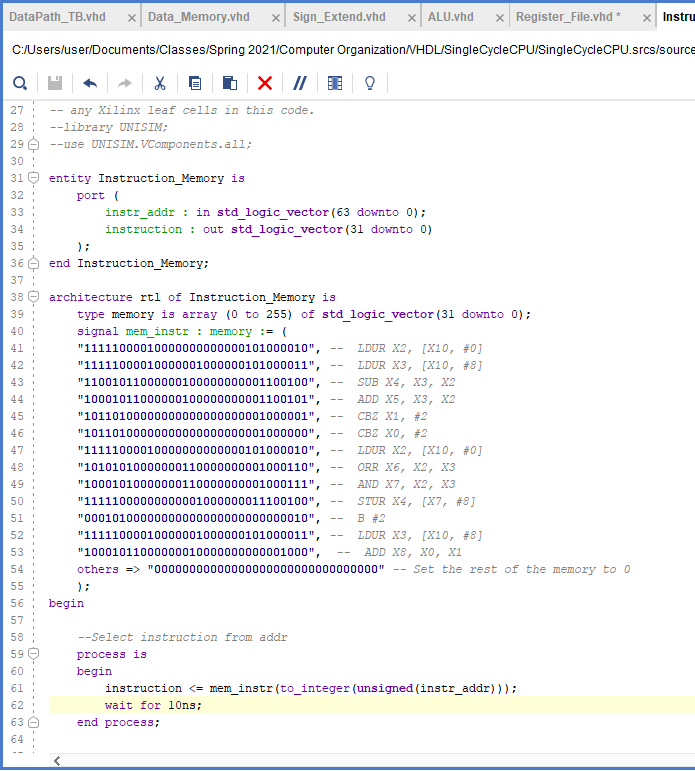


Figure 2. Instruction Memory

* The image above shows the instruction memory for my CPU. It contains 256 memory locations but only has 13 actual instructions in it. The rest are set to all 0s

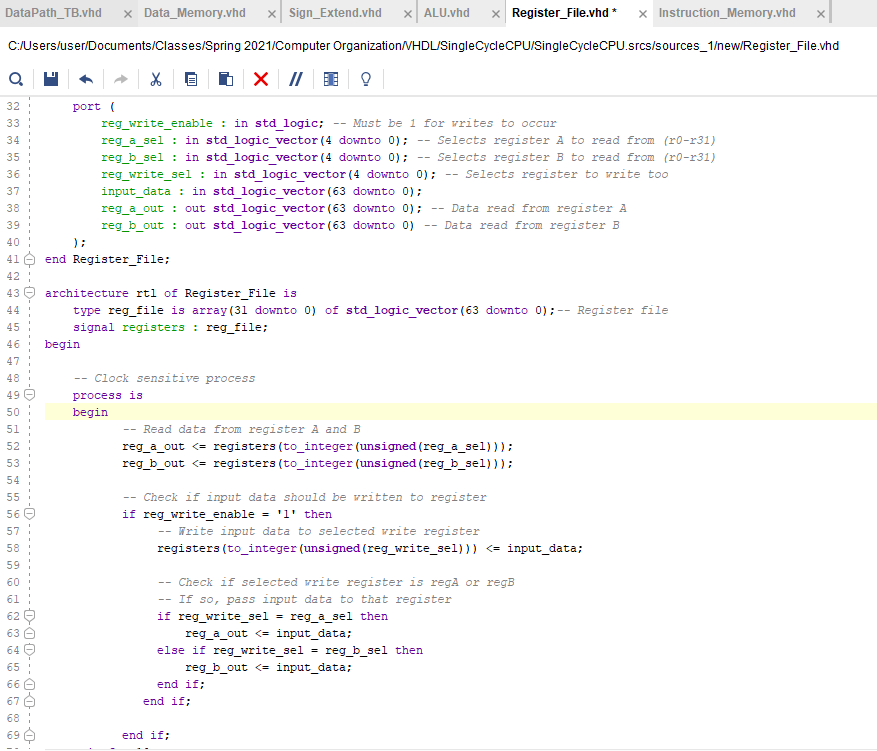


Figure 3. Register File

* This is the register file. It consists of 32 64-bit registers, inline with the LEGv8 standard. It reads the contents of registers a and b and outputs them. If the write\_enabled flag is set, the input data will be written to the selected write register.

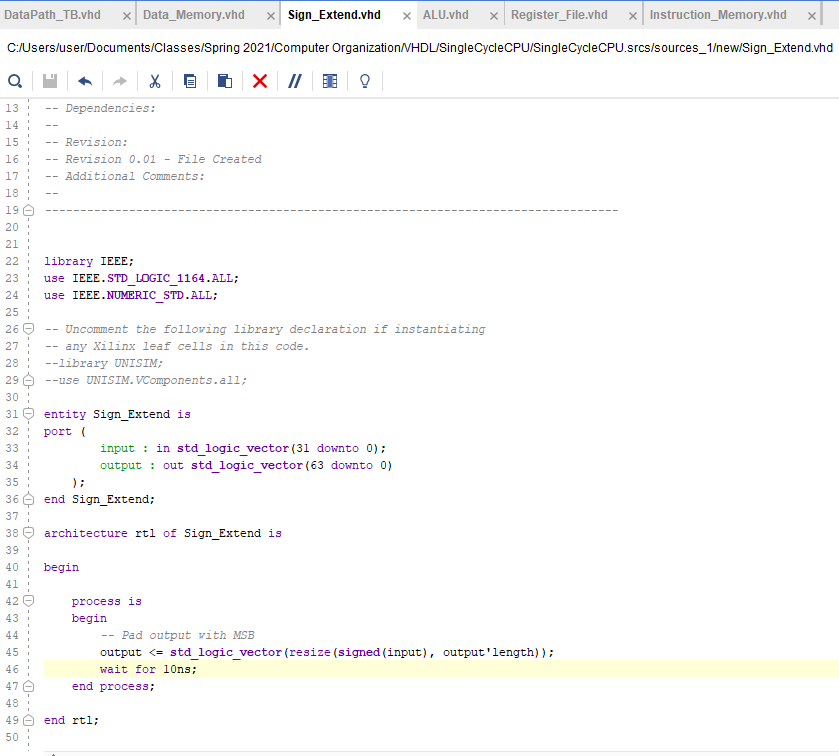


Figure 4. Sign Extender

* This component is by far the simplest. It takes a 32-bit input and sign-extends it to 64-bits based upon its sign bit.

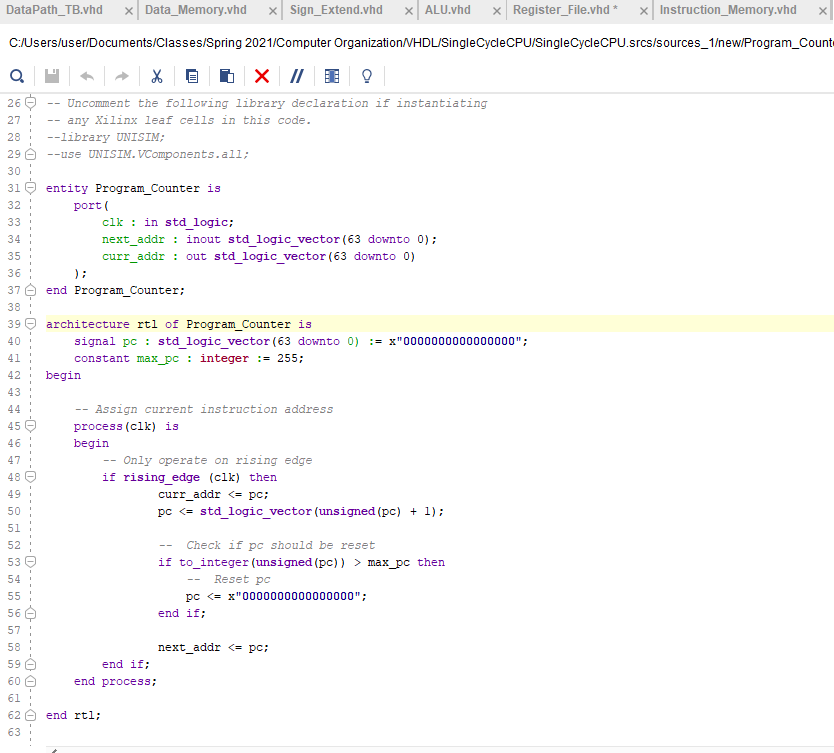


Figure 5. Program Counter

* This is the CPU’s program counter. It begins at 0 and maxes out at 255. The pc is incremented on every rising clock edge. If it exceeds the maximum pc, it is reset to 0.